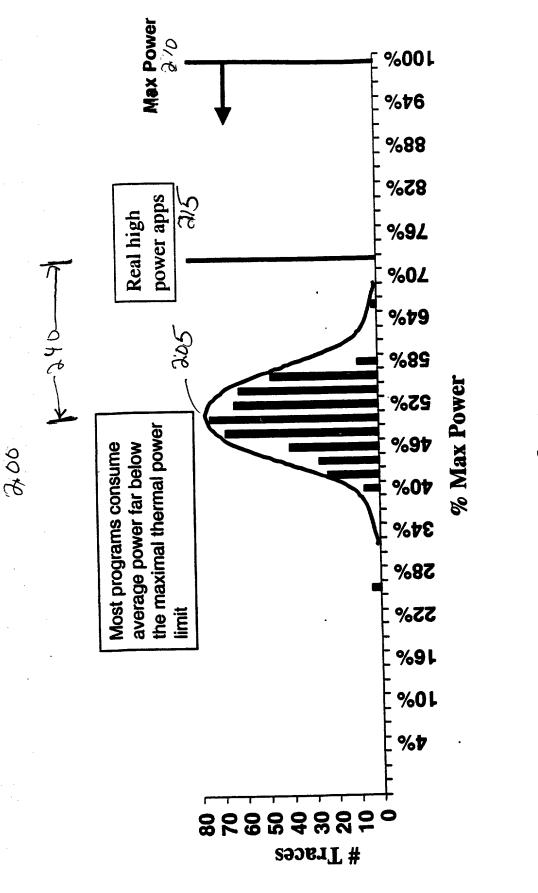


FIG. 1



F56 3

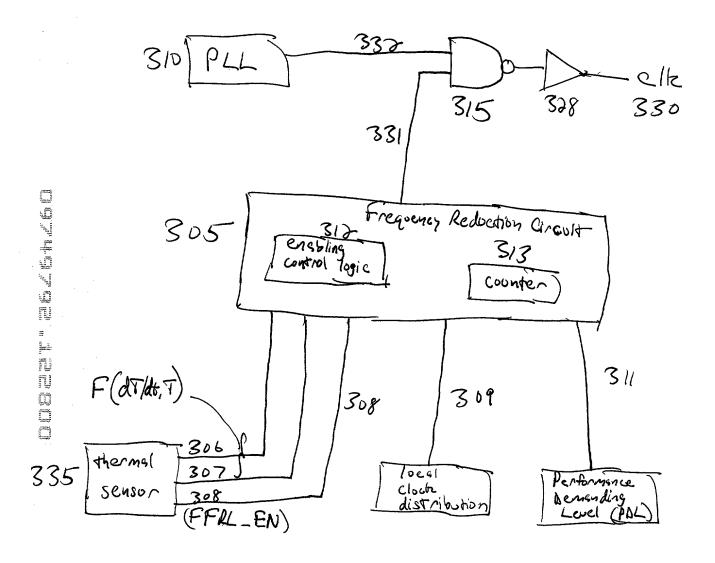


FIG. 3



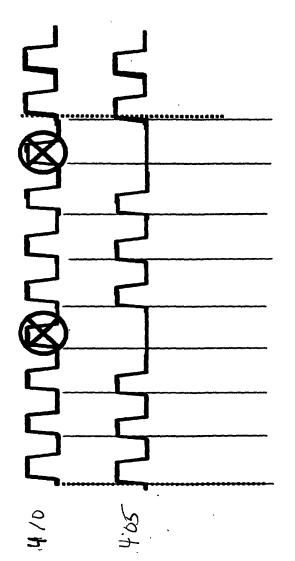
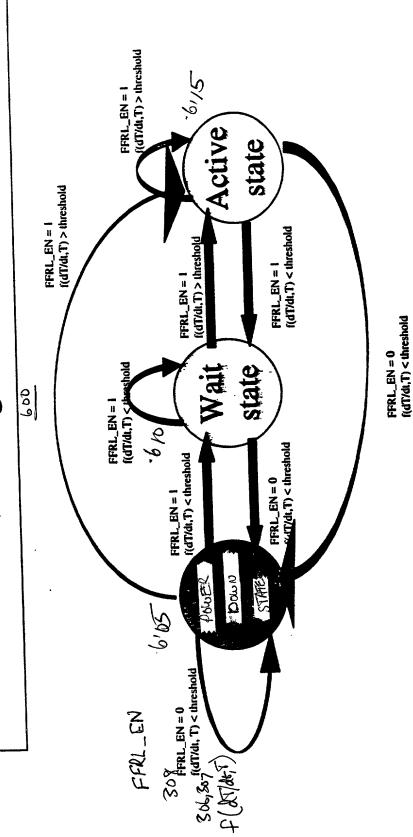


Figure 4.

FFRL_EN	dT/dk	Thermal temperature	Current logic state	Prev. logic state
0 (not near maximal thermal limit)	Not Care	Not Care	Power down	Power down
0 (not near maximal thermal limit)	Not Care	Not Care	Power down	Welt
0 (not near maximal thermal fimit)	Not Care	Not Care	Power down	Active
I (near maximal thermal limit)	<0.2 (slow rate)	<max. -="" 8t<="" td="" temperature=""><td>Power down ···</td><td>Power down</td></max.>	Power down ···	Power down
1 (near maximal thermal limit)	>0.2 (slow rate)	<max. -="" 8t<="" td="" temperature=""><td>Wait</td><td>Power down</td></max.>	Wait	Power down
1 (near maximal thermal limit)	<0.2 (slow rate)	<max. &t<="" -="" td="" temperature=""><td>Power down</td><td>Welt "</td></max.>	Power down	Welt "
1 (near maximal thermal limit)	>0.2 (slow rate)	<max. -="" td="" temperature="" ôt<=""><td>Walt</td><td>Walt .</td></max.>	Walt	Walt .
1 (near maximal thermal limit)	Not Care	>max. temperature - &t	Active	Power down
T (near maximal thermal limit)	Not Care	>max. temperature - 8t	Active	Wait.
1 (near maximal thermal limit)	Not Care	>max. temperature - 8t	Active	Active

FIG 5.

## Logic States Diagram of Fast Frequency Reduction Logic (FFRL)



FFRL\_EN: Fast frequency reduction logic enable signal; Threshold: logic state transite threshold; dT/dt: temperature changing rate; T: thermal temperature; f(dT/dt, T): function of dT/dt and T

Figure 6